12 Volt Wall Outlet for the DC House Project

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Abstract

The purpose of this project is to build a DC-DC converter for the wall outlet of the DC House. This report focuses on the development of the DC -DC converter, and explains the design process as well as summarize the final results. The proposed system using the Buck or Step Down topology takes input voltage of 48V and output 12V at 100W. Results show the ability of the converter to fulfill such task while maintaining efficiency about 90% at all load.

Table of Contents

List of Figures

List of Tables

I. INTRODUCTION

A DC to DC converter is a piece of circuitry that converters one Direct Current voltage level to another DC voltage. These converters are able to transmit power efficiently and over a range of loads. DC to DC converters have a wide range application, and are implemented in a majority of electronic products. Applied largely to computers and cell phones, DC to DC converters allow electronics to have different DC sources for all the purposes necessary. A laptop is an application that cannot operate without DC to DC converters. Voltage from AC outlet first is converted from 110V to a range of 18-24V DC. This voltage is then divided to provide three different output rails: 12V, 5V and 3.3V. 12V rails are used primarily for powering fans, hard drive, and motors. 5V and 3.3V rails are used to power electronic components such as RAM, CPU, chipset and low end video cards. DC-DC converters are also widely used in power distribution.

The purpose of this project is to design and build three separate 48V-12V buck converters that can each deliver power to a 100Watt load. This converter will be used in the DC House project as a wall outlet. An outlet was needed to power appliances that owners of the DC house might possibly use(fans, fridges, stoves etc.).

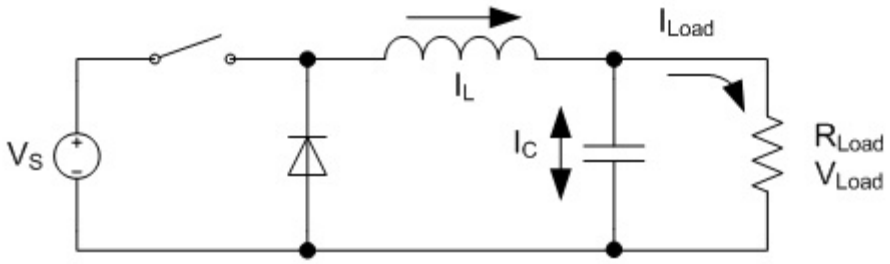


Figure 1-1: General Buck Converter Topology

II. DESIGN REQUIREMENTS

This goal of this project will be to develop an adapter for the wall outlets of the DC house project that will provide the users the ability to use common electrical appliances. The wall outlet will feature a 48V to 12V DC-DC buck converter. Each outlet will have the capacity to deliver 100Watts to various loads. This converter will be designed to handle a maximum load current of 8.33 Amps. These loads include common appliances such as a fan, an electric stove, a 13" black and white television, and a rechargeable battery operated radio. This project will also feature a custom made PC board for the non-isolated topology that was chosen.

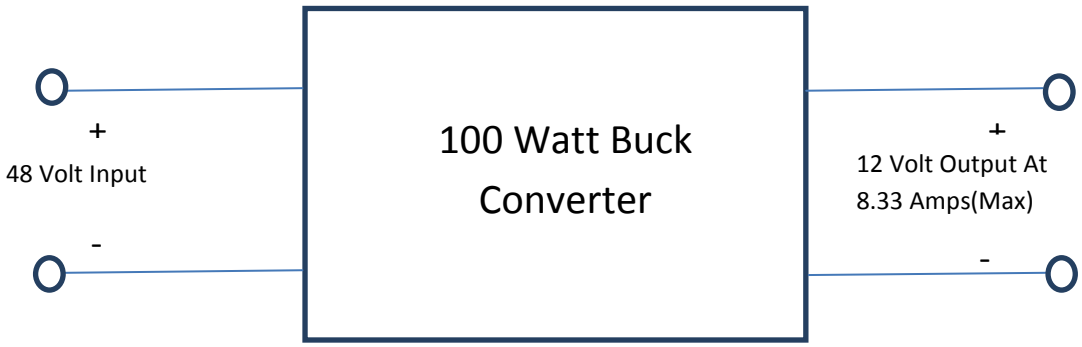


Figure 2-1: Project System Block Diagram

Cost effectiveness and reliability will be the two primary criteria that will dictate the design and implementation of this project. This project will also meet the following specifications:

- Twoworking converters that can deliver 100 Watts of power each
- Output voltage within 5% of 12 Volts.
- Line Regulation under 5%
- Load Regulation under 5%
- Greater than 90% efficiency from 50% load to 100% load

- Output voltage ripple less than 5%
- A plastic housing that allows space for the attachment of an outlet face plate, proper ventilation and insulation for the user

This project will also implement the housing structure for the converter itself that will serve as protection for the user and for the converter from outside disturbances. The outlet will be modelled after two pronged American light sockets. This interface will be able to be easily changed that the user will be able to interface the converter with whatever plug may be necessary.

III. DESIGN AND SIMULATION

Upon researching possible implementations to step down the 48 Volt source to the necessary 12 Volt output, a non-isolated synchronous topology was chosen to increase efficiency and decreases costs that would increase with the use of isolated topologies that implement the use of transformers.

A. COMPONENT SELECTION

Since Linear Technologies provides free simulation software for a majority of the integrated circuits they produce, they were chosen as the first place to begin the search for a suitable switching regulator. With help from a Linear Technology representative the LT3845 was selected as the switching regulator to be used for this project. The through-hole package was selected for ease of soldering during the hardware implementation phase of the project.

Recommended circuit designs in the LT3845 data sheet provided aid in developing a viable circuit diagram. Using the design equations given in the datasheet, a few components were adjusted to achieve the necessary voltage and current outputs. The first components to be changed were resistors R5 and R6, which determine the magnitude of the output voltage. Using the equation below which was provided in the datasheet for output programming, resistor values for R5 and R6 were selected to be 143kΩ and 16.2kΩ respectively.

$$R5 = R6\left(\frac{V_{OUT}}{1.231} - 1\right)$$

Equation 3-1

The Rsense resistor is used to set a maximum current output as related to the equation:

$$R_{Sense} = \frac{70mV}{I_{OUT(MAX)}}$$

Equation 3-2

Given that our maximum output is to be set at 8.33Amps, the equation yielded an Rsense of 8.4mΩ and was rounded down to 8mΩ to easily obtain a resistor with the stated value.

The LT3845 also features an adjustable frequency pin . By setting the resistor attached to pin 3 of the switching regulator to 49.9kΩ the frequency is set to 300kHz. This value was selected due to a table provided in the datasheet that shows various resistor values and switching frequency. The frequency can also be set to a precise value through the equation given in the datasheet that is listed below.

$$R_{SET}(k\Omega) = 8.4 * 10^4 * f_{SW}{}^{(-1.31)}$$

Equation 3-3

MOSFETs with low RDS(ON) values were chosen to minimize losses within the converter and thus increasing efficiency. Affordability also of the MOSFETs was a major factor in selection and design. Each converter will utilize two MOSFETs since a synchronous converter was selected to be used. That being said the NTD5867NL power MOSFETs were chosen due to a RDS(ON) of 39mΩ and their ability to handle up to 18 Amps of current.

Inductor selection also depended on general equations provided in the datasheet. Using a ΔIL of 1.41 Amps, fsw of 300kHz, and the desired input and output values of the converter, a value of 22uH is obtained

$$L > V_{out} * \frac{(V_{IN} - V_{out})}{(f_{SW} * V_{IN} * \Delta I_L)}$$

Equation 3-4

The next component to be selected was the output capacitors which were chosen to reduce the output voltage ripple and clean up the output signal. Three capacitors of value 33uF were chosen to be arranged in parallel to provide adequate filtering of the output signal.

As with the rest of the component selection, values were taken from the provided circuit schematic. These component values were deemed adequate after determining their effect on the circuit. These components make up the signal portion of the schematic.

B. SIMULATION RESULTS

Using LTSpice IV and the provided simulation file, simulations were performed to obtain various data values such as efficiency, load regulation, line regulation, output ripple and the minimum load in which the converter still operates in continuous conduction mode. These simulations were performed using the following circuit schematic.

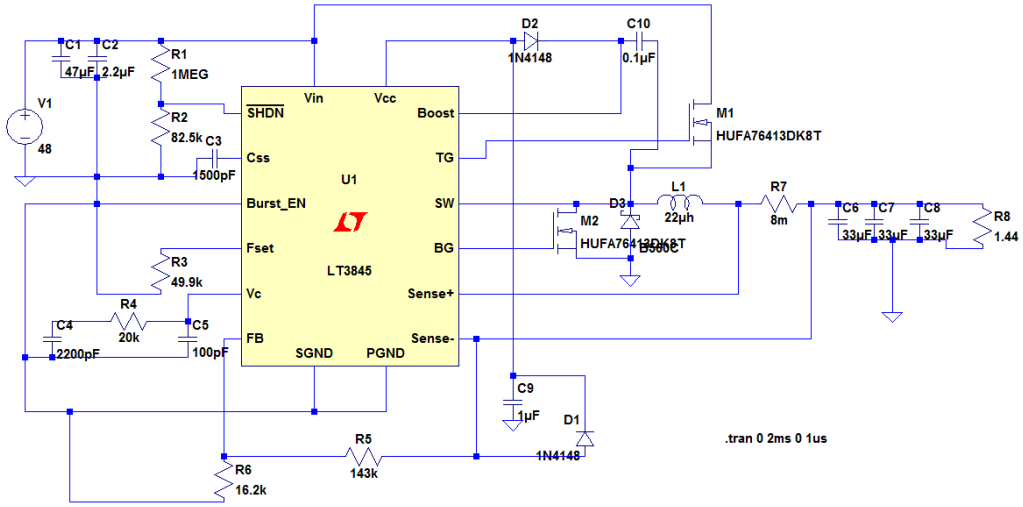


Figure 3-1: Simulated Schematic Diagram

Efficiency test at various loads are performed from 10% to 100% at 10% intervals are performed to obtain a range of efficiency data that can be seen in Figure 3-2 and the tabulated data can be seen in Table 3-1.

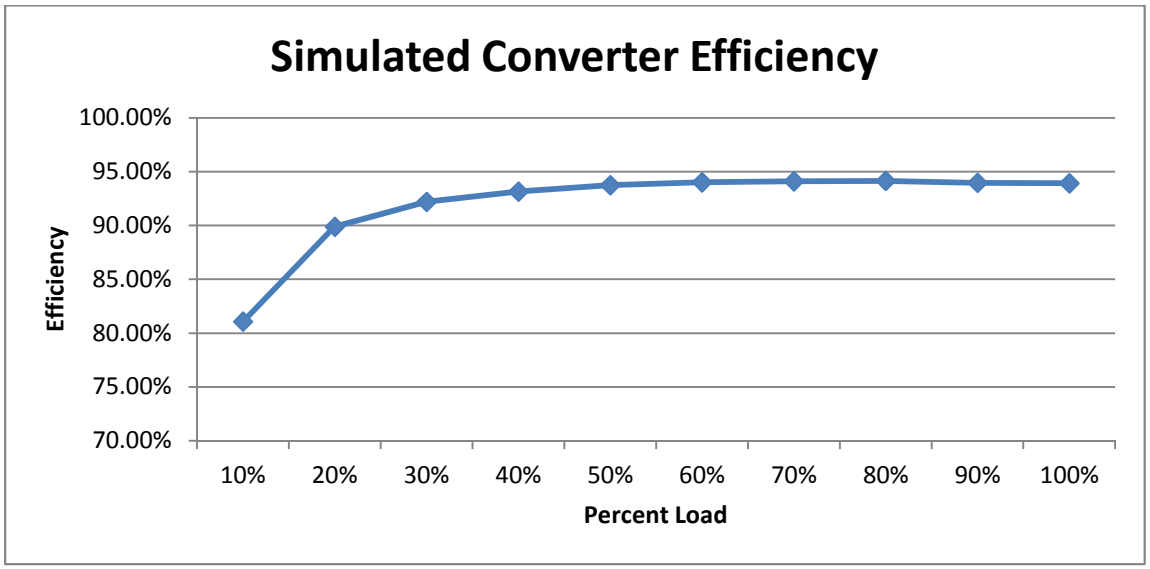


Figure 3-2: Efficiency Data with Varying Loads

Table 3-1: Simulated Converter Data

Load	Pin(Watts)	Pout(Watts)	Iout(Amps)	Efficiency
10%	12.57	10.19	0.84	81.07%
20%	22.61	20.32	1.68	89.87%
30%	33.06	30.48	2.52	92.20%
40%	43.62	40.63	3.36	93.15%
50%	54.18	50.79	4.2	93.74%
60%	64.82	60.94	5.04	94.01%
70%	75.45	71	5.87	94.10%
80%	86.31	81.25	6.72	94.14%
90%	97.21	91.34	7.56	93.96%
100%	108.12	101.54	8.39	93.91%

On top of high efficiencies, the LT3845 also boasts line and load regulations of 0.58% and 0.25% respectively when simulated in LTspice. The converter continues to operate in CCM down to 6% load.

IV. HARDWARE RESULTS

In order to achieve maximum efficiency and ensure that converter performs as well as possible, a custom made circuit board from expressPCB.com. Using the free software from ExpressPCB, the circuit board in Figure 4-1 was developed using the 4 layer board design option provided in the software. The main idea behind the 4 layer board option is to minimize the internal noise caused by the board as well as the simplicity of the layout compared to the 2 layer board option. The benefit of the low noise and the simplified design shifted the final decision towards the 4 layer board design option.

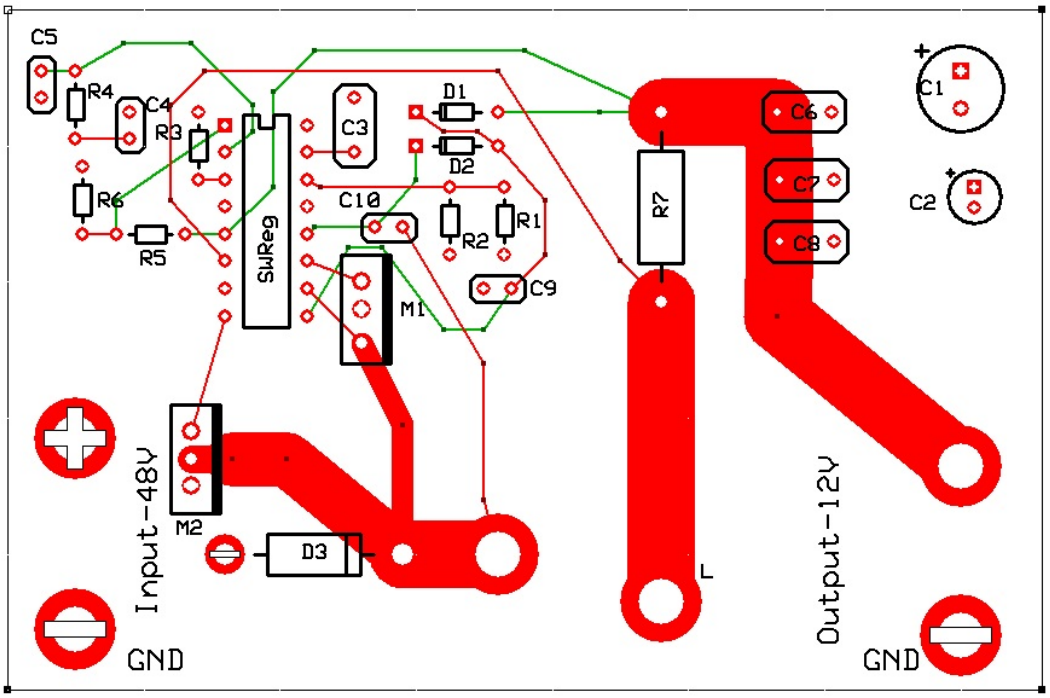


Figure 4-1: PCB Schematic

Using component dimensions provided by Digikey for the parts used in the converter, a custom component dimension was created for the power inductor used in the circuit. The software had several standard component sizes to be used for the rest of the circuit. The PCB also

utilizes separate ground and power planes to reduce interference between the power and ground signals.

Larger traces are used for the power nodes in the design. Specifically the drain pin for M2 and the source pin for M1. The duty cycle of this converter is 25% since VOUT/VIN = 12/48. Since M2 is the synchronous MOSFET placed in parallel with diode D3 and will carry 75% of the total output current during the low part of the duty cycle, the trace need to be 75% as wide as the 0.25" traces for the output. The trace coming from the source pin of M1 will only carry 25% of the total output current, it is sufficient for it to be 25% of the width of the output traces.
The power nodes are placed as far away as possible from the signal nodes to reduce the effect that heat would have on the components responsible for the signals in the converter. The power nodes are also placed away from the switching node on the LT3845. This helps reduce interference that will come from the high power nodes on the circuit.

Using two separate layers to place traces on the circuit board, the signal portion of the converter is preserved for the upper left hand section of the circuit board. This will ensure that there is no cross interference between the two power planes.

Upon receiving the completed PCBs from ExpressPCB, they were soldered together and the board in Figure 4-2 resulted. The pictured circuit board measures 2.75" by 3.5" and did not have any visual defects upon inspection.

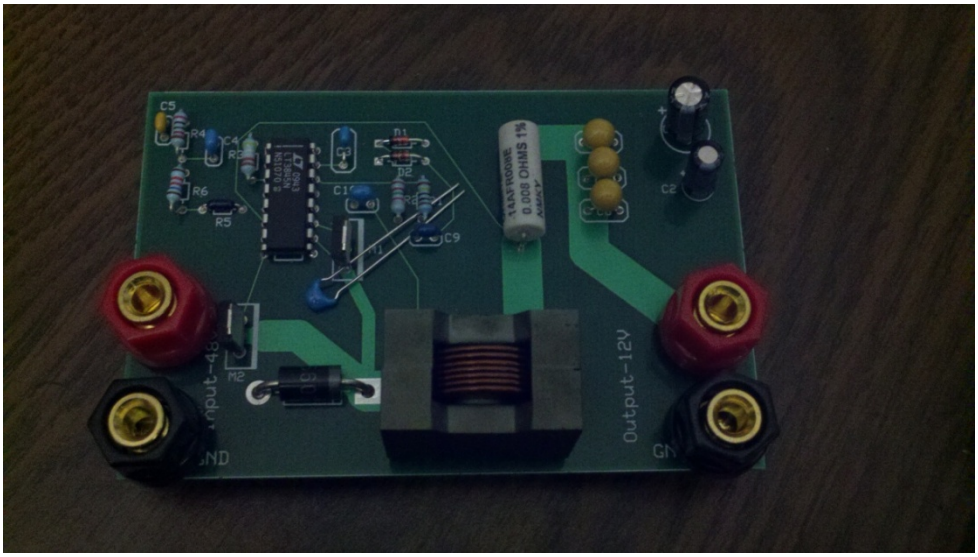


Figure 4 – 2: Soldered PCB

Using power supplies, power meters, multimeters and electronic loads in the power electronics lab, measurements were performed to record the efficiency, line regulation, load regulation, and voltage output ripple.

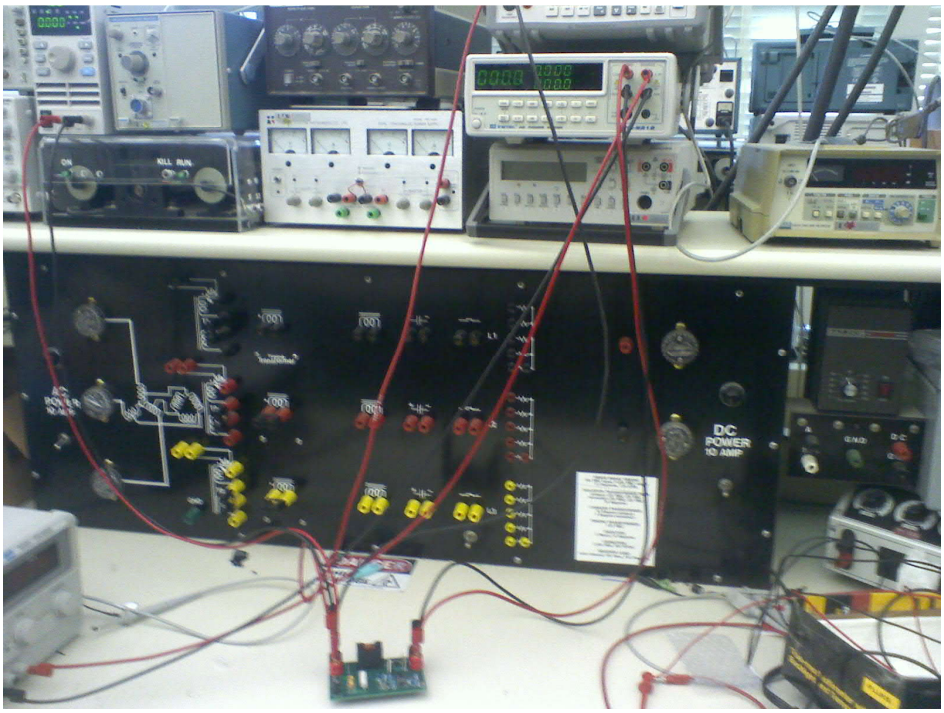


Figure 4-3: Testing Set-Up

Upon testing the first two converters, it was discovered that they were in working order and performed as expected; the third converter however, was not performing as expected. After replacing both the MOSFETs and the LT3845 switching regulator, the circuit was still inoperable. As a result only two working converters were produced for this project.

The two working converters performed according to design requirements, and even exceeding simulated efficiencies with a maximum efficiency at 40% load for converter 1 and 50% load for converter 2. Both the plotted efficiencies can be seen below. The graphs show efficiency as a result of output power. This output power is analogous to percent load sine the maximum output power for the converter is 100 Watts and thus a decrease to 90 Watts in output power results in a 10% step down in output power.

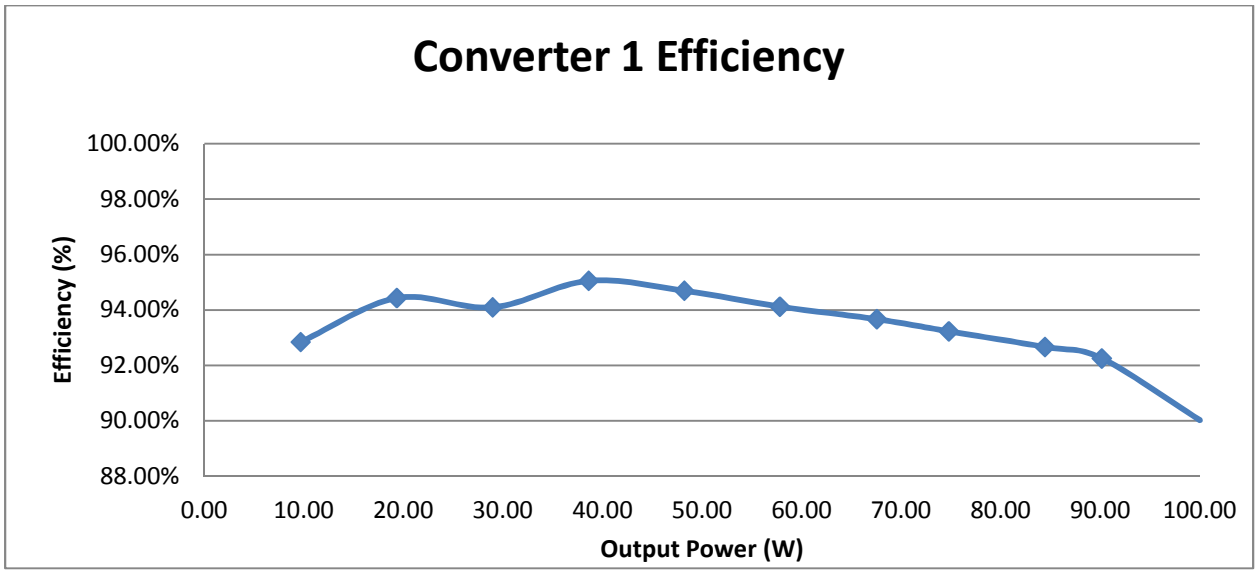


Figure 4-4: Output efficiency of Converter 1

Upon looking at both graphs, it can be observed that converters maintained efficiencies above 90% even down to 10% load. This definitely meets the stated design requirements in chapter II of the report.

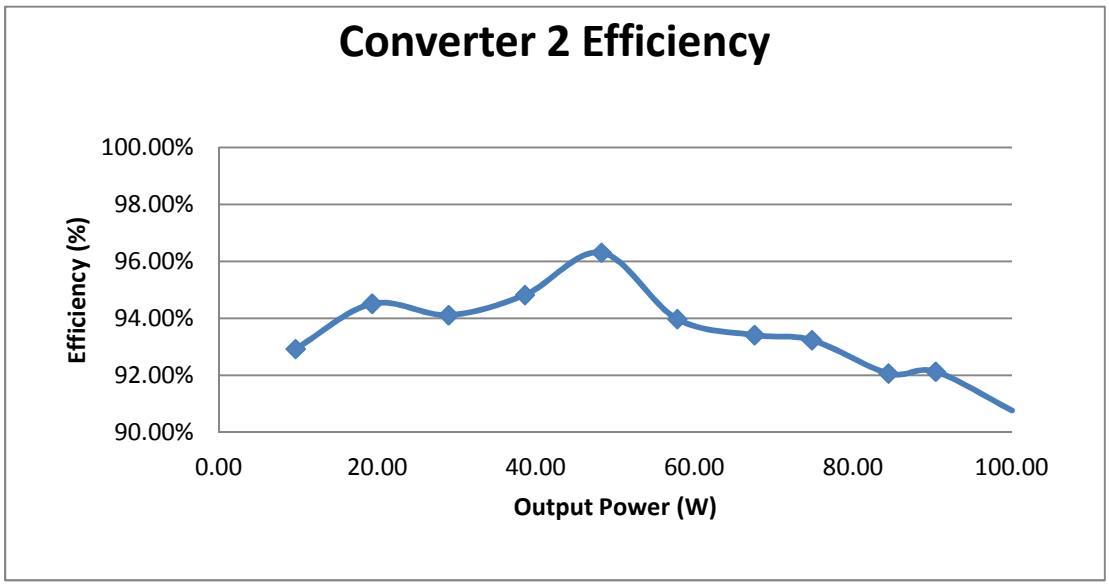


Figure 4-5:Output efficiency of converter 2

Tabulated efficiency data are as follows. As seen in the tables below, the nominal output voltage for each of the converters was 12.05 Volts. This value is 0.417% away from the desired 12.0 Volts of the output. This range also falls into the desired tolerance as stated in the design requirements chapter.

Table 4-1: Converter 1 Efficiency Data

Converter #1	Pin(Watts)	Vout(Volts)	Iout(Amps)	Pout(Watts)	Efficiency
	10.4	12.07	0.8	9.66	92.85%
	20.45	12.07	1.6	19.31	94.44%
	30.76	12.06	2.4	28.94	94.10%
	40.6	12.06	3.2	38.59	95.05%
	50.9	12.05	4	48.20	94.70%
	61.4	12.04	4.8	57.79	94.12%
	72.1	12.06	5.6	67.54	93.67%
	80.2	12.06	6.2	74.77	93.23%
	91.1	12.06	7	84.42	92.67%
	97.7	12.05	7.48	90.13	92.26%
	111.1	12.05	8.3	100.02	90.02%

Table 4-2: Converter 2 Efficiency data

Converter #2	Pin(Watts)	Vout(Volts)	Iout(Amps)	Pout(Watts)	Efficiency
	10.4	12.08	0.8	9.66	92.92%
	20.45	12.08	1.6	19.33	94.51%
	30.78	12.07	2.4	28.97	94.11%
	40.7	12.06	3.2	38.59	94.82%
	50.09	12.06	4	48.24	96.31%
	61.5	12.04	4.8	57.79	93.97%
	72.3	12.06	5.6	67.54	93.41%
	80.2	12.06	6.2	74.77	93.23%
	91.7	12.06	7	84.42	92.06%
	98.1	12.05	7.5	90.38	92.13%
	110.2	12.05	8.3	100.02	90.76%

Table 4-3: Other Output Data

Converter 1	Line Regulation	Load Regulation	Vopp	Vopp(%)
	0.83%	0.23%	260mV	2.17%
Converter 2				
	0.95%	0.25%	300mV	2.50%

The tables above show that line regulation, load regulation and Peak to Peak output ripple were below the specified values in the design requirements chapter.

CONVERTER CASING

A secondary goal or the personal goal that was not listed within the requirement of the project was to make an encasing for the converter that would be integrated into the DC House as a complete outlet set. The encasing must be space efficient as well as to provide openings for input and output of the converter while shielding the converter from possible external damage.

The prototype encasing for the converter is made out of proxy glass purchased from Home Depot. The material was cut by the precision laser cutter in the Mustang 60' machine shop using the program called Adobe Illustrator. The design of the box was done on AutoCAD to make an exact dimension of 5.35 x 4.2 x 3.125 inch. Six sides were cut with matching dimensions. To simplify the joining of the sides, openings were cut onto some of the side itself to allow for insertion of another side. Figure 4-6 below shows the finished product of the encasing.

Figure 4-6: Stand up view of the encasing for the converter

The front side and the back side of the encasing also had square cut by using the Dremel tool. The front side was cut to allow the attachment of the wall socket to connect to the 12V output of the converter. The back side of the encasing was cut to allow wires from 48V source to attach to the input of the converter. Figure 4-7 shows a better view of the front and back side of the encasing.

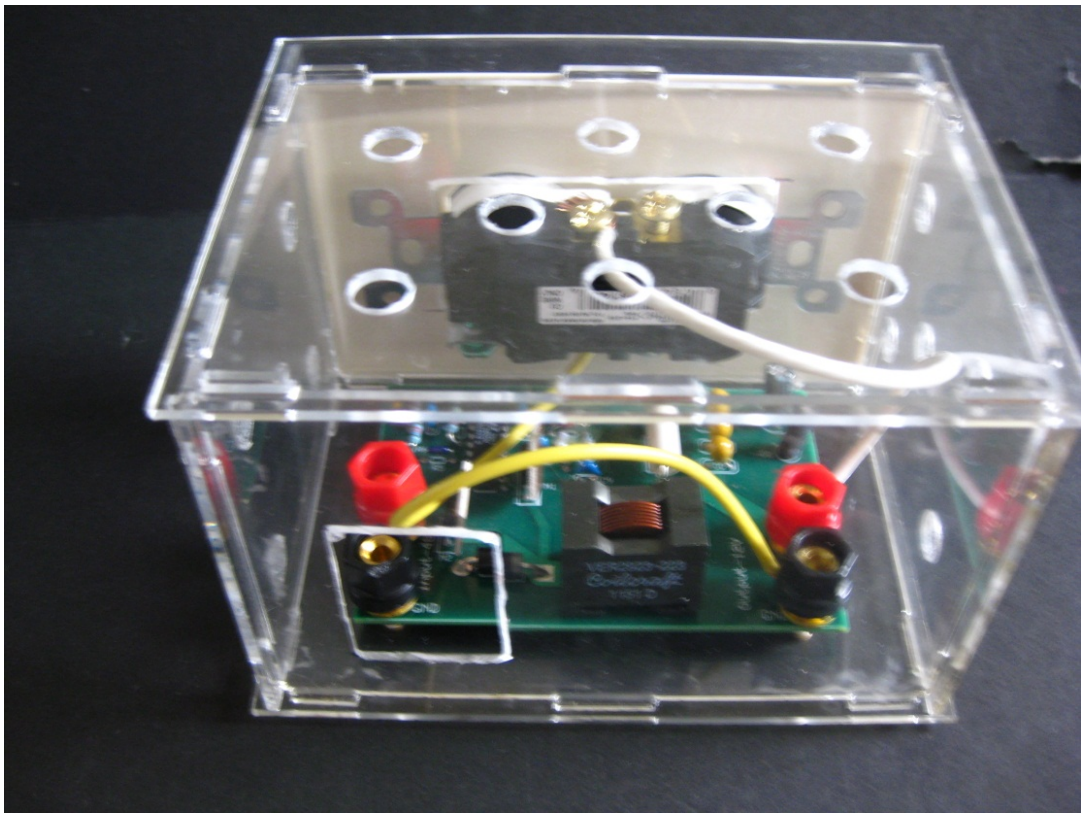


Figure 4-7: Side view of the encasing for the converter

The encasing also had holes drilled on the top, bottom, and sides to allow for ventilation and heat dissipation from the converter. As promised, no external material was used to join the sides of the encasing and it fulfills the goal of protecting the converter.

V. CONCLUSION

The end of result of the converter is fully functional. The converter surpasses the desired values from what was required, keeping efficiency close to the simulation and above 90% efficiency from 50% to 100% load. That being said, at least two of the three built converters were fully functional. While diagnosing the converter, an unforeseen short caused by human error when trying to find the Oscilloscope waveform of a MOSFET resulted in an output capacitor to explode. This caused further breakdown as the team try to replace both the MOSFET and the LT3845 Chip. Unfortunately the desoldering process damages the board and after a careful observation, scratches were found on the tracing path. The team finally ruled out the last converter, leaving it an unsuccessful attempt for trying to achieve the three functional converters dream.

One of the converters was sent to another DC House project group to be field tested with their portion of the project. The converter was connected and displayed live during the Senior Project Exhibition in Spring 2012. The converter provided 12V output for the DC appliances without showing any signs of breakdown. The main components, such as the MOSFETS and the Chip, that must tolerate and handle the most current showed some signs of overheating. As one of the next steps for further work, a heat sink should be attached to each of the MOSFET and the Chip.

Another future work would be to place a fuse onto the board to prevent shorting the circuit and damaging the board. As the team learned the hard way from the testing stage with the third converter, it provided an important learning experience for dealing with high current applications. If a fuse had also been placed at the output stage, in series with the inductor of the circuit, then the output capacitor of the third converter would not have exploded and the converter may continue to be diagnosed for problems instead of a broken board. Furthermore, different topology could be built and tested to check for even higher efficiency converter.

Overall, the proposed 48-12V DC-DC converter design was a success. Two of the three built converters had desired output figures with low load and line regulation, all of which are under 1% compared to the required 5%. The goal for this project was to build a wall outlet for the bigger DC House Project, and the converter built illustrated the ability to fulfill the desired output voltage of 12V to provide to DC appliances.

APPENDIX A

Buck Converter Parts list

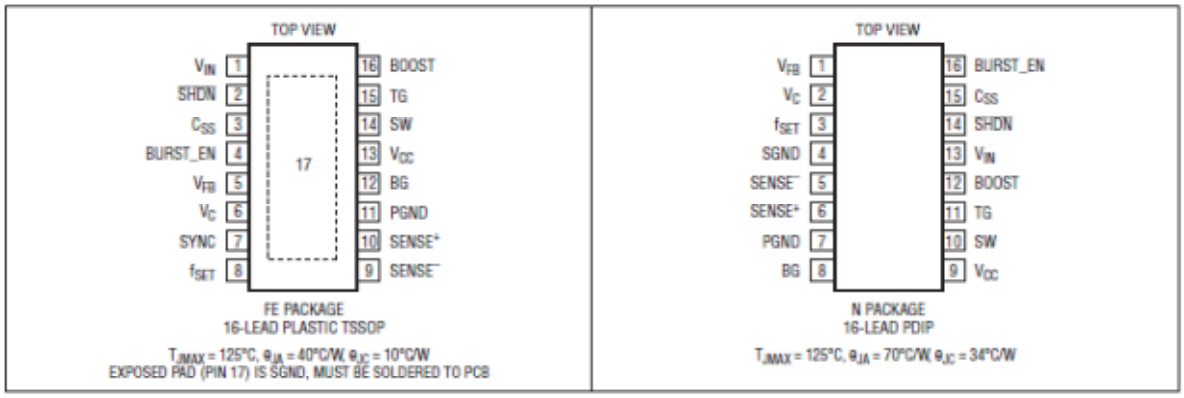
Component	Digikey#	Component Value	Price	Quantity Needed	Total Price
C1	SH470M050ST-ND	47uF	0.16	4	0.64
C2	338-2343-ND	2.2uF	0.28	4	1.12
C3	490-5358-ND	1500pF	0.3	4	1.2
C4	490-3779-ND	2200pF	0.31	4	1.24
C5	BC1015CT-ND	150pF	0.41	4	1.64
C6	478-6064-ND	33uF	1.33	4	5.32
C7	478-6064-ND	33uF	1.33	4	5.32
C8	478-6064-ND	33uF	1.33	4	5.32
C9	445-5315-ND	1uF	0.43	4	1.72
C10	490-3810-ND	0.1uF	0.23	4	0.92
R1	RNF14FTD1M00CT-ND	1M	0.15	4	0.6
R2	RNF14FTD82K5CT-ND	82.5k	0.15	4	0.6
R3	RNF14FTD49K9CT-ND	49.9k	0.15	4	0.6
R4	RNF14FTD20K0CT-ND	20k	0.15	4	0.6
R5	CMF143KQFCT-ND	143k	0.49	4	1.96
R6	RNF14FTD16K2CT-ND	16.2k	0.15	4	0.6
R7	14AFR008E-ND	8m	1.98	4	7.92
D1	1N4148FS-ND	-	0.14	4	0.56
D2	1N4148FS-ND	-	0.14	4	0.56
D3	641-1420-1-ND	-	0.5	4	2
L1	Coilcraft	22uH	0	4	0
SWReg	LT3845EN#PBF-ND	-	7.13	5	35.65
M1	NTD5867NL-1GOS-ND		0.56	5	2.8
M2	NTD5867NL-1GOS-ND		0.56	5	2.8
				Total	**81.69**

APPENDIX B

Valuable Selections from the LT3845 Data Sheet

1. Pin Configuration

PIN CONFIGURATION



2. Pin Functions

PIN FUNCTIONS

TG: The TG pin is the bootstrapped gate drive for the top N-Channel MOSFET. Since very fast high currents are driven from this pin, connect it to the gate of the power MOSFET with a short and wide, typically 0.02" width, PCB trace to minimize inductance.

V_C: The V_C pin is the output of the error amplifier whose voltage corresponds to the maximum (peak) switch current per oscillator cycle. The error amplifier is typically configured as an integrator by connecting an RC network from the V_C pin to SGND. This circuit creates the dominant pole for the converter regulation control loop. Specific integrator characteristics can be configured to optimize transient response. When Burst Mode operation is enabled (see Pin 4 description), an internal low impedance clamp on the V_C pin is set at 100mV below the burst threshold, which limits the negative excursion of the pin voltage. Therefore, this pin cannot be pulled low with a low impedance source. If the V_C pin must be externally manipulated, do so through a 1kΩ series resistance.

V_{CC}: The V_{CC} pin is the internal bias supply decoupling node. Use a low ESR, 1µF or greater ceramic capacitor to decouple this node to PGND. Most internal IC functions are powered from this bias supply. An external diode connected from V_{CC} to the BOOST pin charges the bootstrapped capacitor during the off-time of the main power switch. Back driving the V_{CC} pin from an external DC voltage source, such as the V_{OUT} output of the regulator supply, increases overall efficiency and reduces power dissipation in the IC. In shutdown mode this pin sinks 20µA until the pin voltage is discharged to 0V.

V_{FB}: The output voltage feedback pin, V_{FB}, is externally connected to the supply output voltage via a resistive divider. The V_{FB} pin is internally connected to the inverting input of the error amplifier. In regulation, V_{FB} is 1.231V.

V_{IN}: The V_{IN} pin is the main supply pin and should be decoupled to SGND with a low ESR capacitor (at least 0.1µF) located close to the pin.

Exposed Pad (SGND) (TSSOP Only): The exposed leadframe is internally connected to the SGND pin. Solder the exposed pad to the PCB ground for electrical contact and optimal thermal performance.

PIN FUNCTIONS

BG: The BG pin is the gate drive for the bottom N-channel MOSFET. Since very fast high currents are driven from this pin, connect it to the gate of the power MOSFET with a short and wide, typically 0.02" width, PCB trace to minimize inductance.

BOOST: The BOOST pin is the supply for the bootstrapped gate drive and is externally connected to a low ESR ceramic boost capacitor referenced to SW pin. The recommended value of the BOOST capacitor, C_{BOOST}, is at least 50 times greater than the total gate capacitance of the topside MOSFET. In most applications 0.1µF is adequate. The maximum voltage that this pin sees is $V_{IN} + V_{CC}$, ground referred.

BURST_EN: Burst Mode Operation Enable Pin. This pin also controls reverse-current inhibit mode of operation. When the pin voltage is below 0.5V, Burst Mode operation and reverse-current inhibit functions are enabled. When the pin voltage is above 0.5V, Burst Mode operation is disabled, but reverse-current inhibit operation is maintained. In this mode of operation (BURST_EN = V_{FB}) there is a 1mA minimum load requirement. Reverse-current inhibit is disabled when the pin voltage is above 2.5V. This pin is typically shorted to ground to enable Burst Mode operation and reverse-current inhibit, shorted to V_{FB} to disable Burst Mode operation while enabling reverse-current inhibit, and connected to V_{CC} pin to disable both functions. See Applications Information section.

C_{SS}: The soft-start pin is used to program the supply soft-start function. Use the following formula to calculate C_{SS} for a given output voltage slew rate:

$$C_{SS} = 2\mu A(t_{SS}/1.231V)$$

The pin should be left unconnected when not using the soft-start function.

f_{SET}: The f_{SET} pin programs the oscillator frequency with an external resistor, R_{SET}. The resistor is required even when supplying external sync clock signal. See the Applications Information section for resistor value selection details.

PGND: The PGND pin is the high-current ground reference for internal low side switch driver and the V_{CC} regulator circuit. Connect the pin directly to the negative terminal of the V_{CC} decoupling capacitor. See the Application Information section for helpful hints on PCB layout of grounds.

$SENSE^-$: The $SENSE^-$ pin is the negative input for the current sense amplifier and is connected to the V_{OUT} side of the sense resistor for step-down applications. The sensed inductor current limit is set to ±100mV across the SENSE inputs.

$SENSE^+$: The $SENSE^+$ pin is the positive input for the current sense amplifier and is connected to the inductor side of the sense resistor for step-down applications. The sensed inductor current limit is set to ±100mV across the SENSE inputs.

SGND: The SGND pin is the low noise ground reference. It should be connected to the $-V_{OUT}$ side of the output capacitors. Careful layout of the PCB is necessary to keep high currents away from this SGND connection. See the Application Information section for helpful hints on PCB layout of grounds.

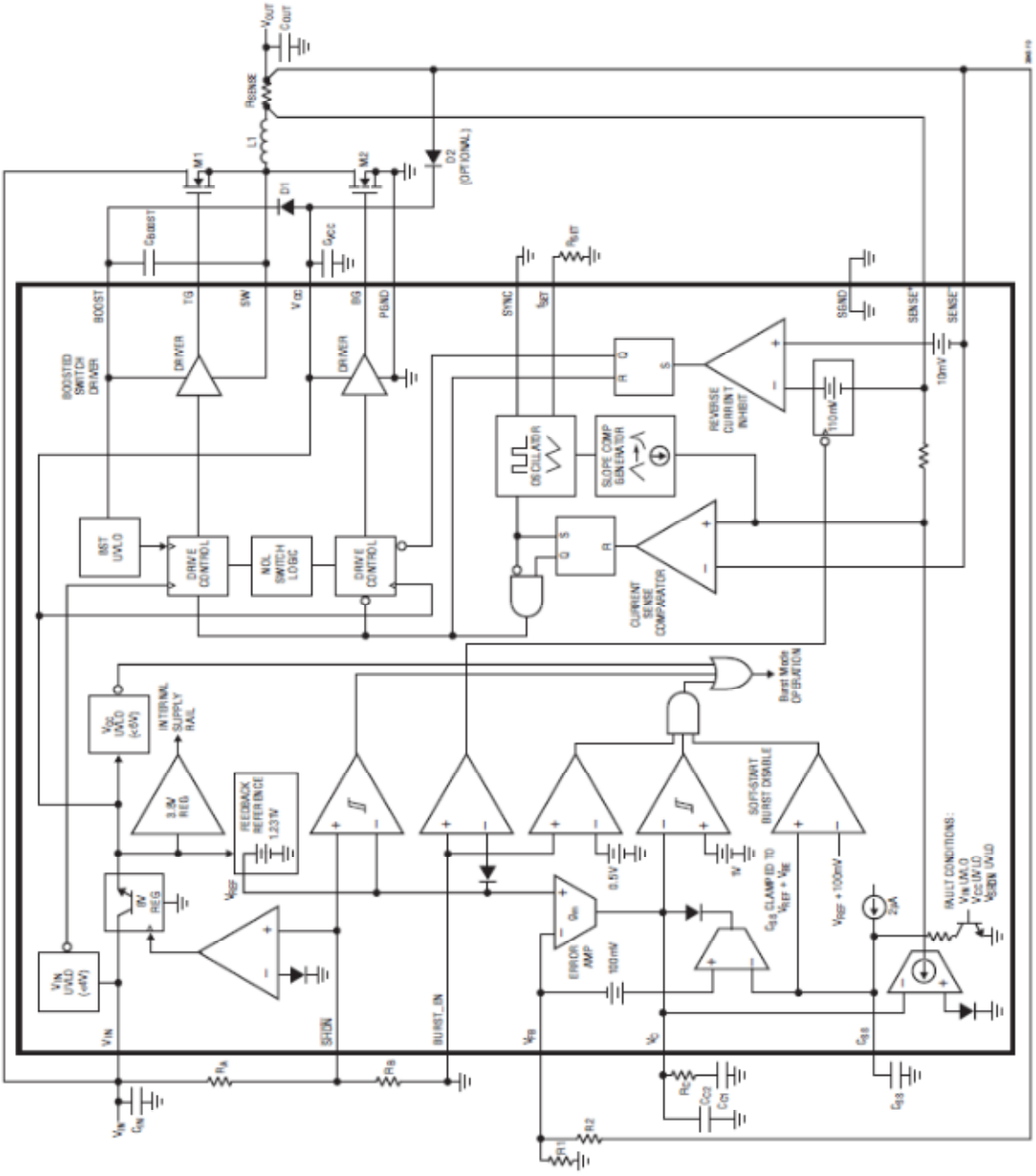
$\overline{SHDN}$: The $\overline{SHDN}$ pin has a precision IC enable threshold of 1.35V (rising) with 120mV of hysteresis. It is used to implement an undervoltage lockout (UVLO) circuit. See Application Information section for implementing a UVLO function. When the $\overline{SHDN}$ pin is pulled below a transistor V_{BE} (0.7V), a low current shutdown mode is entered, all internal circuitry is disabled and the V_{IN} supply current is reduced to approximately 9µA. Typical pin input bias current is <10nA and the pin is internally clamped to 6V. If the function is not used, this pin may be tied to V_{IN} through a high value resistor.

SW: Reference for V_{BOOST} Supply and High Current Return for Bootstrapped Switch.

SYNC: The Sync pin provides an external clock input for synchronization of the internal oscillator. R_{SET} is set such that the internal oscillator frequency is 10% to 25% below the external clock frequency. If unused the Sync pin is connected to SGND. For more information see "Oscillator Sync" in the Application Information section of this data sheet. Sync pin not available in PDIP package.

3. LT3845 System Block Diagram

BLOCK DIAGRAM



4. Design Equations

Table 1. Recommended 1% Standard Values

R_{SET} (kΩ)	f_{SW} (kHz)
191	100
118	150
80.6	200
63.4	250
49.9	300
40.2	350
33.2	400
27.4	450
23.2	500

$$R_{SENSE} = \frac{70mV}{I_{OUT(MAX)}}$$

$$R_{SET(k\Omega)} = 8.4 \bullet 10^4 \bullet f_{SW}^{(-1.31)}$$

$$L_{MIN} > V_{OUT} \bullet \frac{2DC_{MAX} - 1}{DC_{MAX}} \bullet \frac{R_{SENSE} \bullet 8.33}{f_{SW}}$$

$$L \geq V_{OUT} \bullet \frac{V_{IN(MAX)} - V_{OUT}}{f_{SW} \bullet V_{IN(MAX)} \bullet \Delta I_L}$$

$$R2 = R1\left(\frac{V_{OUT}}{1.231V} - 1\right)$$